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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

paper No. 14

Application Number: 09/127,085

Filing Date: July 31, 1998

Appellant(s): Paul E. McKenny

Pryor A. Garnett

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 16, 2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is not correct.

The status of all claims are :

1. Claimed canceled: None
2. Claims withdrawn from consideration but not canceled: None
3. Claims pending: 1-6

(4) Status of Amendments

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The grouping of claims as stated by appellant is not correct. The correct grouping of the claims are as follow:

Patentability of claim 1 stands alone.

Patentability of claim 2 stands alone.

The Patentability of claims 4-6 stand or fall with the patentability of claim 3.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is substantially correct. In the Appendix, the Appealed claims are claims 1-6.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,727,209	Slingwine et al.	Mar. 10, 1998
4,916,697	Roche et al.	Apr. 10, 1990

(10) New Prior Art

No new prior art has been applied in this examiner's answer.

(11) Grounds of rejection.

The following grounds of rejection are applicable to the appealed claims:

The text of those sections of Title 35, US Code not included in this office action can be found in a prior Office Action.

In the final office action issued on 6/04/2001;

(I) Claims 2-6 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01.

For example the preamble of claim 2 recite "physical memory", and "data structure". There is no relationship between any of these elements and the means or steps of the claims. Knowing that "**physical memory**" is used to distinguish between actual **RAM** and "**logical**" or "**virtual**" memory, it is not clear whether "**memory**" in line 17 (claim as originally filed) is the same as "**Physical memory**" in line 14. It is unclear "the data structure" on line 15, stores a number of current generation of its node or number of current generation for every other node (See the next statement in the claim: "data structure comprising a variable stored in the memory of each node and ..."). In other words, is there **one data structure for all the nodes** or **every node has its own data structure**. As another example, in claim 3 (as originally filed), line 25, the "**data structure on a processor's node**" determines if all other processor's node have passed through a quiescent state, then in line 27, the claim recite "**indicating in a data structure accessible to all nodes**".

Is it the same data structure recited on line 25. If so, the step on line 27-29 is the repeat of the previous step.

Claims 4-6 are rejected because of the rejection of their parent claims.

(II)

Claims 1-6 are rejected under 35 U.S.C. § 103 as being unpatentable over Slingwine (U.S.Pat No. 5,727,209) in view of Roche et al. (U.S.Pat No. 4,916,697).

As per claim 1-3, Slingwine, teaches:

- of **multi processor** (See Abstract, **multi processor**, col. 2, lines 8-19), having **interconnected processing nodes** (Fig, 3, **elements 108, and 110**), each with one or more processor and physical memory (col. 6, lines 51-58, also Fig. 4, processors); data structure for storing execution history (Fig. 4, execution history, and summary of execution history col. 8, lines 31-35), **states of threads** that are used for providing mutual exclusion between current and next generation data element (quiescent state of thread and generation, col. 7, lines col. 18-24, and Quiescent state and mutual exclusion, col. 7, lines 50-68, also **mutual exclusion overhead, and a generation data structure**, col. 7, lines 18-46);

first level bit containing bit per node (hierarchical per-thread bitmap is a data structure maintains a hierarchy of bits, where the **next level maintain one bit per group of threads** [Ex. Interpretation: say processor or node of processors], col. 9, lines 30-44); and , a second level bit containing a bit per processor (lowest level maintain one bit per thread, col. 9, lines 30-44).

While the reference of Slingwine teaches of hierarchical bitmap, i.e. bit per thread and bit per group of threads, he fail to explicitly teaches of **bit masks**. However, it is well known in the art at the time invention was made to use **level bit mask** for the indication of passing through a quiescent state, as it is evidenced by Roche et al. (Each bit in the sculpture register 72 has an associated bit in two or three mask register, ...Col. 8, line 5-30). Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use "**level bit mask** registry as an indication of a state of a processor" of Roche, in the multi exclusion and concurrency method of Slingwine et al.

Per claim 2, Slingwine teaches of a data structure for storing a variable containing current generation number in col. 11 , lines 53-58 (relockgen: **a generation counter that tracks a**

global generation number, See also global next generation and per processor generation in col. 11, lines 29-38).

Regarding claim 3, Slingwine teaches of Generation Data Structure in col. 7, lines 25-30 (data structure that tracks a **particular generation element, and system-wide, per data structure, per group of data structure**).

Regarding claims 4-6 and the limitation of callback processor checking is the processor has passed through a quiescent state and indicating that in the data structure, the reference of Slingwine et al. teaches of **a CALLBACK PROCESSOR 100, and a CALLBACK PROCESSOR 104** which is an element of a generation data structure, and an entity that monitors a summary of thread activity 106 (col. 6, lines 36-50).

(12 New Ground of Rejection

Examiner's Answer does not contain any new ground of rejection.

(13) Response to argument

At the outset, Examiner would like to clear that the Amendment after finale (Amendment B), filed on September 6, 2001,

has not been entered. As it is clear from the advisory action issued on November 21, 2001, the Amendment after final raises new issue which requires new search (See, paper number 6, markup version of Amended claims, last paragraph in claim 2, and the insertion of "first", "second", and "third" before the "data structure" in claim 3). As it is clearly stated in the Advisor Action, dated November 21, 2001, the Amendment after Final, raises new issue that requires further consideration and/or search. Therefore, it is not entered.

Applicant on page 4 of his argument states "*clearly other Amendments were also made to place the application in better condition for appeal*". Examiner totally disagree. In response, Applicant's attention is respectfully directed to the fact that these kind or arguments relates to petitionable subject matter under 37 CFR 1.181 and not to appealable subject matter. See MPEP § 1002 and § 1201.

The amendment while trying to clarify some of the 35 USC 112 second paragraph issues, add limitations which requires new search by examiner. It is not clear, why appellant is trying to add new limitations which has not been searched into the claims and insisting that they place the application in better condition

for Appeal. On the subject of Claims 7-10 in the aforementioned Amendment, these claims are totally new and have not been examined. How can one argue about the patentability of claims which is not entered and have not been examined by the Examiner (See, page 9 of the argument).

On page 4, last Paragraph Appellant argue "The Examiner refused to enter the amendment after final because the addition of language to claim 3 regarding the first, second, and third data structures (see advisory action dated 11/21/02). However, applicants were amending claim 3 specifically to overcome the 112 rejection by the Examiner. In the Final Office action at page 3, the Examiner indicated that it was unclear whether a recited data structure was the same data structure as a previous data structure or a different one ("Is it the same data structure recited online 25", Office action at page 3). Applicants simply amended claim 3 to clarify that they may be different data structures. Consequently, the amendment should have been entered."

In response, it is submitted that, having one data structure on a node for keeping track of the states of the threads (single and or group), with three data structure possibly on different locations is totally different and considered new issue. Even with three data structure as claimed in the Amendment which is not entered, it is unclear whether the third data structure, is on a single node or is global to all the nodes, for example shared memory.

On page 6, Appellant argue, *"The Examiner seems to focus on the preamble of the claim and argues that Slingwine teaches "states of threads" and a "summary of thread activity." (Final Office action, page 3). However, the body of the claim calls for the first level and second level bit masks to indicate whether the processor has not yet passed through a quiescent state. For this part of the claim, the Examiner argues it is well known at the time of the invention to use level bit masks for an indication of passing through a quiescent state. (Final Office action, page 4, citing Roche at Col. 8, lines 5-30). However, the portion of Roche the Examiner cites has nothing to do with indicating whether a node contains a processor that has not yet passed through*

a quiescent state. Nor does Roche teach a bit per processor associated with a particular node, the bit indicating whether the corresponding processor has not yet passed through a quiescent state.

Rather, Roche specifically states that "the associated bits indicating into which levels the particular error is to be classified." (Roche, 8:5-8). The remaining portion of Roche from Col. 8,

lines 5-30, clearly indicates that Roche is discussing error detection, not whether or not a processor has passed through a quiescent state. Thus, the Examiner's decision to reject claim 1 should be reversed."

In response, it is submitted that, Applicant argues the patentability of claims by individually addressing the references used to reject the claims. It is noted that the claims above are rejected as being obvious using a combination of the references. Applicant can not show non-obviousness by attacking the references individually where as here the rejections are based on a combination of references, **In re Keller,** 208 USPQ 871 (CCPA 1981). The reference of Slingwine, teaches of the "bit per node" and "bit per processor" in **hierarchical per-thread bitmap is a data structure maintains a hierarchy of bits, where the next level maintain one bit per group of threads (col. 9, lines 30-44); and , a second level bit containing a bit per processor (lowest level maintain one bit per thread, col. 9, lines 30-44).** The reference of Roche is used primarily to show **level bit mask** is used for the indication of passing through a quiescent state (See, section 11 (II) of this Examiner's Answer).

On page 7-8, Appellant argue *"Claim 2 requires a data structure stored in the physical memory on each node for storing a number of the current generation of data elements being processed by a processor on a node. The Examiner makes almost no mention of any specific limitations of*

claim 2. In fact, Applicants specifically pointed out in an amendment dated March 19, 2001, that "the Examiner did not demonstrate any reasoning for finding claims 2 or 3 obvious..." (Response of March 19, 2001, at page 5).

Nonetheless, the Examiner continues to provide limited reasoning for rejecting claim 2. Claim 2 requires a data structure stored in the physical memory on each node, which Slingwine does not disclose. Additionally, claim 2 has been amended to further remove it from Slingwine by requiring that "the current generation number on the nodes are updated in lockstep so the nodes have local access...". Slingwine does not store the current generation on each node and thus would have no reason to update the current generation number in lockstep on the nodes. Thus, the Examiner's decision to reject claim 2 should be reversed."

In response, Examiner disagree. First, Appellant is arguing about a limitation which is not in the claims (See, Amendment a). There is no recitation of "stored in the physical memory of each node" in the claims. Secondly, Applicant should read the references by its entirety. The reference of Slingwine teaches of bit per node and bit per group of threads on col. 9 (See, section 11 (II) of this Examiner's Answer).

On page 8-9, Appellant argue "*Applicants respectfully request reversal of the Examiner's rejection of claim 3.*

Claim 3 has numerous limitations that the Examiner does not appear to address. For example, claim 3 requires "determining from a first data structure on the processor's node if the processor has passed through a quiescent state." The Examiner does not appear to address this language in the rejection.

Nor does the Examiner mention or point out where in the references the following language of claim 3 is disclosed: "if so, determining from a second data structure on the processor's node if all other processors on its node have passed through a quiescent state."

Nor does the Examiner mention or point out where in the references the following language of claim 3 is disclosed: "if so, indicating in a third data structure accessible to all nodes that all processors on the processor's node have passed through a quiescent state."

Applicants believe it is the Examiner's burden to show why the invention is not patentable. Applicants requested the Examiner to more specifically identify where the above limitations are found in the references, but have received essentially the same rejection again with no particulars identified."

In response, Applicant's attention is directed to the teaching of Slingwine, in col. 7, lines 25-30 (data structure that tracks a **particular generation element, and system-wide, per data structure, per group of data structure**). See Slingwine, col. 10, lines 6-17, where he teaches of "Any thread accessing the data structure must execute special-case steps in response to the per-thread bit such as recording its quiescence before accessing the data structure".

(14) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Majid A. Banankhah

MAJID BANANKHAH
PRIMARY EXAMINER